ELECTRICAL PERFORMANCE EVALUATION FOR MULTI-CHIP ASSEMBLIES USING KNOWLEDGE BASED APPROACH [1]

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Summary

In this paper, preliminary work on electrical performance estimation and evaluation for multi-chip assemblies (i.e., multi-chip modules , chip on board, and etc.) is presented. A knowledge base is built to facilitate system performance merits evaluation process. Even though many other parameters can be included in the performance merit set, at this stage only electrical performance merits such as module frequency, module size and power dissipation are modeled. The other performance merits (e.g., cost estimation, thermal resistance and reliability, and etc.) are to be included in future work.

Four major design/technology catagories of inputs were incorporated into the models to calculate the module frequency, module size, and power dissipation. The analytical formulas applied in this work were verified against our more exact solution tools developed in the University of Arizona. These equations are refined until model predictions are within acceptable tolerance of error. Initial four major groups are:

1. Interconnect technology: cross section geometry of the interconnection, thin film or thick film technology, substrate dielectric constants.

2. Logic technology: CMOS or nMOS technology, on chip delay estimation, detailed output driver delay estimation.

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3. Building chip information for the module: this includes the number of chips, effective chip area, chip frequency Fc, and the number of I/O's for each chip.

4. Bonding technology: flip chip, wire bonding, and tab bonding.

Prior to final assembly of a system product, it is essential to understand the performance merits. This is because selecting a particular technology/interconnect design may result in more profitable product than its counterpart. This specific tool can be an asset to a MCM designer at early stages to verify his or her performance merits for different (applicable to one's company) technology/interconnect designs. An artificial intelligence approach can be very useful to guide MCM designers to select a technology/interconnect design that globally optimizes all performance merits.

A knowledge based environment called KROS (Knowledge Representation for Object-Oriented Simulation) with FRASES[1] (Frames and Rules Associated System Entity Structure) is used to organize our knowledge for MCM design and performance evaluation. Our knowledge is represented by a tree-like structure, with sets of selection rules associated with each decision node, and a set of synthesis rules for our final system configuration (i.e., parameters in our four catagories of inputs).

As the number of catagories for each input parameter, and number of performance merits considered for the evaluation increase, each input dependency of the final module performance merits becomes more and more complex. Artificial Intelligence and knowledge–based techniques are necessary to estimate/evaluate different possible technology/interconnect designs without time consuming detailed simulations.

The knowledge base developed for MCM performance evaluation is based on several sets of analysis, testing, simulations and verifications. This work was compared with those of H.B. Bakoglu's[2] and P. A. Sandborn's[3] on performance

merit evaluation. We also discuss why knowledge based approach is essential for future multi–chip assembly systems.

References

[1] Hu, J., Huang, Y. M., and J. W. Rozenblit, "FRASES – A knowledge Representation Scheme for Engineering Design, *Advances in AI and Simulation, SCS Simulation Series*, vol. 20, no. 4, 1989, pp. 141–146.

[2] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Chap.9, Addison-Wesley Publishing Company, New York, 1990.

[3] Peter A. Sandborn, " A software tool for Technology Tradeoff Evaluation in Multichip Packaging", *Proceedings 1991 IEMT Symposium,* September, 1991.